What is claimed is:

1. A method of measuring the phase or frequency of a periodic input signal using a periodic reference signal, comprising:

comparing the input signal to the reference signal to obtain a lead signal and a lag signal; and

changing the count of an up/down counter in dependence on the input signal, the reference signal, the lead signal and the lag signal; and

using the lead signal, the lag signal and the count signal to produce a phase or frequency signal, including:

forming from the lead and lag signal a difference signal;

filtering the difference signal to produce a filtered signal; and

adding to the filtered signal a correction signal of a magnitude determined in accordance with the count signal.

2. The method of Claim 1, wherein the difference signal is filtered to produce an aliased output signal.

3. The method of Claim 2, wherein the aliased output signal has added to it a correction signal representing a positive or negative phase increment to form an unwrapped output signal.

5. Apparatus for measuring the phase or frequency of a periodic input signal using a periodic reference signal, comprising:

a comparison circuit for comparing the input signal to the reference signal to obtain a lead signal and a lag signal;

a logic circuit, including an up/down counter, responsive to the input signal, the reference signal, the lead signal and the lag signal to change the count of the up/down

counter; and

means for using the lead signal, the lag signal and the count signal to produce a phase or frequency signal, including:

means for forming from the lead and lag signal a difference signal;

means for filtering the difference signal to produce a filtered signal; and

means for adding to the filtered signal a correction signal of a magnitude determined in accordance with the count signal.

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8. The apparatus of Claim 6, wherein the means for forming and means for filtering comprise a pulse combiner/filter, and the pulse combiner/filter filters the difference signal to produce an aliased output signal.

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9. The apparatus of Claim 6, wherein the adder adds to the aliased output signal a correction signal representing a positive or negative phase increment to form an unwrapped output signal.

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8. The apparatus of Claim 7, further comprising circuitry for forming the correction signal using the count of the up/down counter.

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9. The apparatus of Claim 8, wherein the circuitry for forming the correction signal comprises a multiplier having as one input signal a constant value and having as another input signal the count of the up/down counter.